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Request for grant of a patent

(See the notes on the back of this form. You can also get an explanatory leaflet from the Patent Office to help you fill in this form)

1.	Your reference 29 JUN 2002	AVH/P01802UK
2.	Patent application number *(The Patent Office will fill in this part)*	0215089.4
		01JUL02 E729755-3 D00291 P01/7700 0.00-0215089.4
3.	Full name, address and postcode of the or of each applicant *(underline all surnames)*	Power Innovations Limited Manton Lane Bedford MK41 7BJ United Kingdom
	Patents ADP number *(if you know it)*	07380694001
	If the applicant is a corporate body, give the country/state of its incorporation	UK
4.	Title of the invention	Overvoltage Protection
5.	Name of your agent *(if you have one)*	**Lewis & Taylor**
	"Address for service" in the United Kingdom to which all correspondence should be sent *(including the postcode)*	**144 New Walk** **Leicester** **LE1 7JA**
	Patents ADP number *(if you know it)*	**711002** ✓

6.	If you are declaring priority from one or more earlier patent applications, give the country and the date of filing of the or each of these earlier applications and *(if you know it)* the or each application number	Country	Priority application number *(if you know it)*	Date of filing *(day / month / year)*

7.	If this application is divided or otherwise derived from an earlier UK application, give the number and filing date of the earlier application	Number of earlier application	Date of filing *(day / month / year)*

8.	Is a statement of inventorship and of right to grant of a patent required in support of this request? *(Answer 'yes' if:* *a) any applicant named in part 3 is not an inventor, or* *b) there is an inventor who is not named as an applicant, or* *c) any named applicant is a corporate body.*	Yes

9. Enter the number of sheets for any of the following items you are filing with this form. Do not count copies of the same document

Continuation sheets of this form	
Description	6
Claim(s)	1
Abstract	0
Drawing(s)	2 + 2

10. If you are also filing any of the following, state how many against each item.

Priority documents	
Translation of priority documents	
Statement of inventorship and right to grant of a patent *(Patents Form 7/77)*	
Request for preliminary examination and search *(Patents Form 9/77)*	One
Request for substantive examination *(Patents Form 10/77)*	
Any other documents *(please specify)*	

11. I/We request the grant of a patent on the basis of this application.

Signature Lewis L Taylor Date 28 June 2002

12. Name and daytime telephone number of person to contact in the United Kingdom: HALLAM Arnold Vincent (0116) 233 8181

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Title: Overvoltage protection

The present invention relates to an overvoltage protection device.

Digital data links and the supporting circuitry often operate with signal levels less than 5OV. These circuits must be protected from electrical interference that can induce much higher voltages into the signal lines which may then cause damage to the circuits. These overvoltages can arise from induced currents from power lines and from lightening discharges. The induced currents can have rise times ranging from less than a microsecond for lightening discharges to many milliseconds for induced mains currents.

There are a wide range of semiconductor devices which are designed to provide protection and many of these are based on a four layer PNPN structure which switches quickly from a blocking state to a high conduction state when the voltage cross the device exceeds a predetermined threshold or breakover voltage. Once the surge current has decayed, the PNPN device reverts back to its non-conducting state.

The present invention seeks to provide an improved semiconductor component.

Accordingly, the present invention provides a semiconductor component suitable for limiting transient voltages on the supply lines of a system having at least three supply lines, one of the supply lines being a current sink, the semiconductor comprising first, second and third overvoltage-triggered semiconductor protection units, wherein a first electrode of each protection unit is connected to a common node having overvoltage breakdown conduction characteristics in one direction and diode conduction characteristics in the other.

The present invention is further described hereinafter, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a sectional view of a first form of conventional semiconductor component for limiting transient voltages, suitable for protecting digital circuitry;

Figure 2 is a diagrammatic representation showing the use of three devices of Figure 1 arranged to protect a digital circuit;

Figure 3 is a sectional perspective view of the arrangement of three components of Figure 1 in a single integrated circuit; and

Figure 4 is a view similar to that of Figure 3 of a preferred form of device according to the present invention.

Referring firstly to Figure 1, this shows a conventional structure of a PNPN device 10 for protecting digital circuitry. Three such devices 10 are shown in Figure 2 in an arrangement suitable for protecting a digital circuit 12.

The device of Figure 1 is fabricated on an N type substrate 14. The substrate has upper and lower surfaces into which two P type base regions 20, 22 are diffused. Heavily doped N type emitter regions 24, 28 and breakdown regions 26, 30 are diffused into the upper and lower surfaces and electrical connection to the device 10 is made through upper and lower metallisations 32.

The voltage at which the device 10 switches into breakdown is defined by the emitter-base junction between the base 20, 22 and the adjacent emitter breakdown region 26, 30. The breakdown voltage can be varied by varying the doping concentrations in the junction region, enabling breakdown voltages in the range 5 to 50 volts to be achieved.

The base regions 20, 22 penetrate through the associated emitter region 24, 28 by way of emitter breakdown shorting dots 34, 36 and 38, 40.

The current path A through the device 10 prior to breakdown is via the forward biassed PN junction between the base region 22 and the substrate 14, between the substrate 14 and the breakdown region 26, through the base region 20 under the emitter region 24 at C and finally out of the emitter shorting dot 34. When the voltage drop along the emitter region at C is enough to forward bias the emitter junction, the device switches into its ON state.

Figure 2 shows three such devices 10 arranged in a star formation to provide protection to two data lines 42, 44 connected to the circuit 12. As can be seen, in practise protection is required between both data lines 42, 44 and ground and therefore three such devices 10 would be required to provide full protection for the circuit 12.

Rather than having three separate devices 10 to provide protection, it is often more convenient to use a single semiconductor component. It is possible to assemble three individual devices in one package but it is much simpler and cheaper to have a single integrated circuit that performs the function of three individual protectors 10.

Figure 3 shows a semiconductor component 100 which incorporates three devices 10 of Figure 1. Like parts with Figure 1 are given like reference numbers.

In the arrangement of Figure 3 a PN diode is formed in each device 10 between the P type base region 20 and a further N type diffusion region 102 formed in the N type substrate 14 at the lower surface of the semiconductor chip 100.

The data lines 42, 44 and ground are connected to the metallisations 30a, 30c and 30b respectively. The metallisation 32 on the lower surface of the semiconductor chip has no external connections and serves to interconnect the devices 10.

If we assume that ground is positive relative to the data lines 42, 44 the pre-breakdown current follows the same path as shown in Figure 1, the path being labelled A in Figure 3. Initial triggering

then occurs through the PN diode formed by the P type base 20b and the N type diffusion 102b. The current passes through the metallisation 32c and then through the emitter breakdown region 26c, the P type base region 20c and the shorting dot 34c. Once enough current flows to switch the PNPN section of the device the current then takes the route D which is directly through the N substrate 14, the P type base region 20c and the emitter region 24c.

The devices 10a, 10b and 10c all operate in a similar manner to provide overvoltage protection in all pluralities.

The type of device illustrated in Figure 3 provides efficient protection for power line and lightening surges with rise times of several microseconds. However, under faster current rise time conditions, it has been found with this type of device construction that the surge capability is degraded. For example, where one might expect a surge capability of 100A the actual surge capability provided under fast current rise time conditions can be as low as 50A. This loss of surge capability arises because the fast rise in voltage across the PN diode formed between the P type base region 20 and the N type diffusion 102 causes a voltage overshoot, resulting in tens of volts being dropped across the diode section. This gives rise to charge carriers building up in the body of the semiconductor and causes the triggering current for the PNPN section to flow in undesirable paths.

A typical unwanted triggering path is shown in dotted lines E in Figure 3 where the current passes through the metallisation 30b, the P type base region 20b, the emitter breakdown region 26c, through the P base region 20c under the emitter region and out through the shorting dot 34. With tens of volts dropped vertically across the PN diode during the diode rise time, the triggering current takes the path of least resistance and in this example, the current flows laterally and does not pass through the N type diffusion 102b and the P type base region 22c of the adjacent device 10c. Since the lateral diode formed by the P type base region 20b and the emitter breakdown region 26c has a lower current capability than that of the diode formed between the P base region 20b and the N type diffusion 102b, the surge rating of the component will be reduced. Intermediate triggering current paths can be formed depending on the current rise time and this does

give unpredictable surge capability to the semiconductor component 100. The surge capability of the component is also reduced for a given area of emitter 24.

The undesirable lateral current flows can be reduced in the component 100 by increasing the separation between the devices 10. However, this is undesirable since it increases the size of the component and thus its cost.

Referring now to Figure 4, this shows a preferred form of semiconductor component 200 according to the present invention. The component of Figure 4 is similar to that of Figure 3 and has three devices 10 constructed in a similar manner to those of Figure 3. However, the component 200 has a respective P shielding diffusion formed between adjacent pairs of devices 10. These completely eliminate the potential unwanted triggering current paths and as a result reduce the degradation of surge capability during fast current rise time conditions.

Since the shielding diffusions 50 are only required to prevent lateral current flow under fast surge condition there is no need to surround each device 10 in a "bucket" of P diffusion, as is the case in a conventional isolation, thus saving chip area.

The preferred form of the invention provides a low voltage semiconductor device (less than 50v) for protecting digital circuitry from transient voltages, the components using a lateral switching mechanism. The component makes use of lateral turn on whilst preventing the surge degradation which can occur as a result of parasitic current paths.

The isolation or shielding diffusions 50 of the component of Figure 4 is a not a full isolation wall and is not designed to support significant voltage drops. It is present between adjacent devices 10 and is designed only to block the parasitic lateral current flows which would otherwise degrade the surge capability of the component. The shielding diffusions only need to be deep enough to impede parasitic current flow sufficiently to ensure that the devices switch on properly. Although in Figure 4 the shielding diffusions 50 are shown extending the full depth of the semiconductor block, each

shielding diffusion 50 may comprise two diffusion portions which extend into the semiconductor block respectively from the upper and lower surfaces but do not meet in the body of the semiconductor block. In this particular case this allows shorter diffusion times and saves silicon area.

The advantage of using the illustrated diffusions 50 over providing a full isolation for each device 10 is a reduction in the silicon area required to achieve the same surge current rating as can be achieved with the conventional component of Figure 3. Thus, a larger surge rating may be achieved in the same area of silicon when compared to a fully isolated device.

The surge capability of the component is provided by the vertical currents.

CLAIMS

1. A semiconductor component suitable for limiting transient voltages on the supply lines of a system having at least three supply lines, one of the supply lines being a current sink, the semiconductor comprising:

first, second and third overvoltage-triggered semiconductor protection units, having overvoltage breakdown conduction characteristics in one direction and diode conduction characteristics in the other; wherein:

a first electrode of each protection unit is connected to a common node;

wherein each said semiconductor protection unit uses a lateral turn on current;

and a shielding diffusion is provided between adjacent units for blocking lateral current flow between adjacent units.

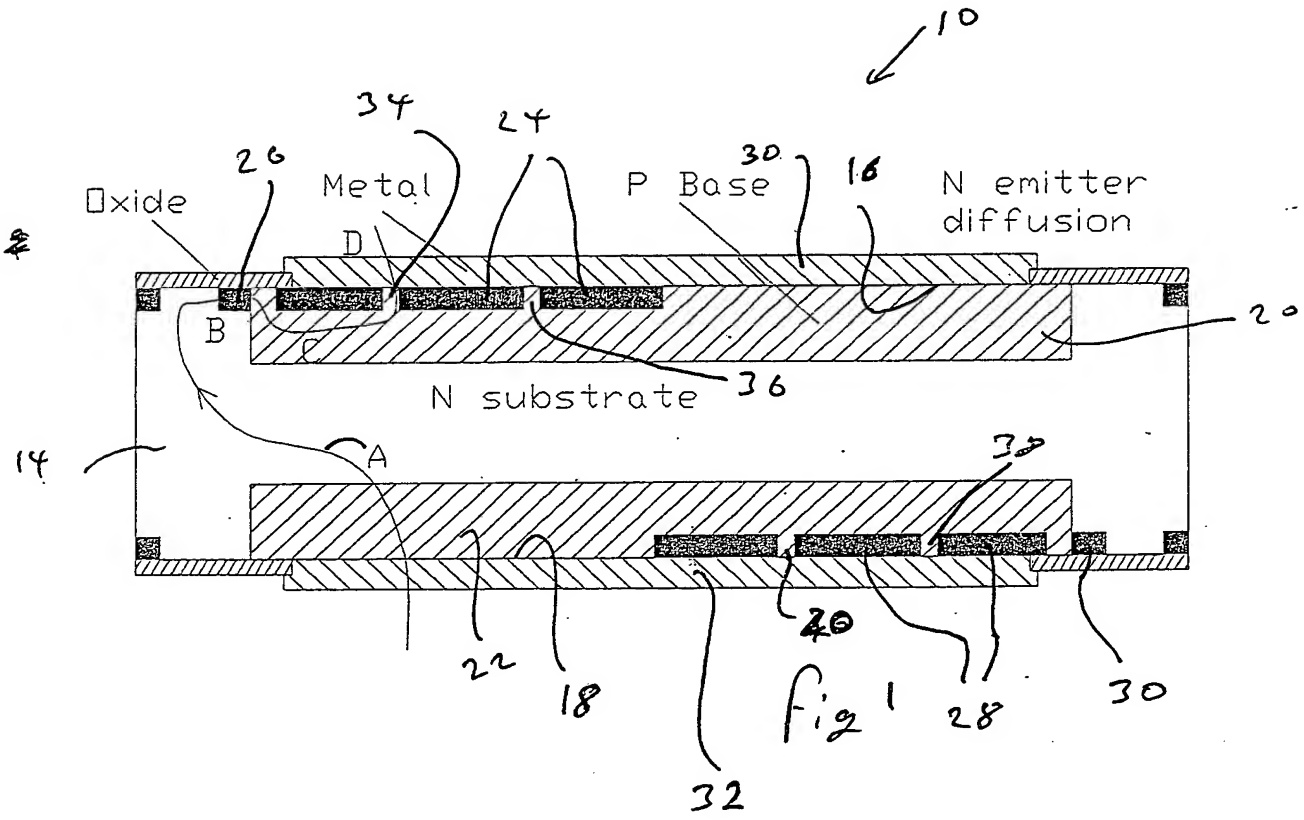
10
34
24
26
Oxide
Metal
P Base
30
16
N emitter diffusion
D
B
C
20
36
N substrate
14
A
38
40
22
18
28
30
32

Fig 1

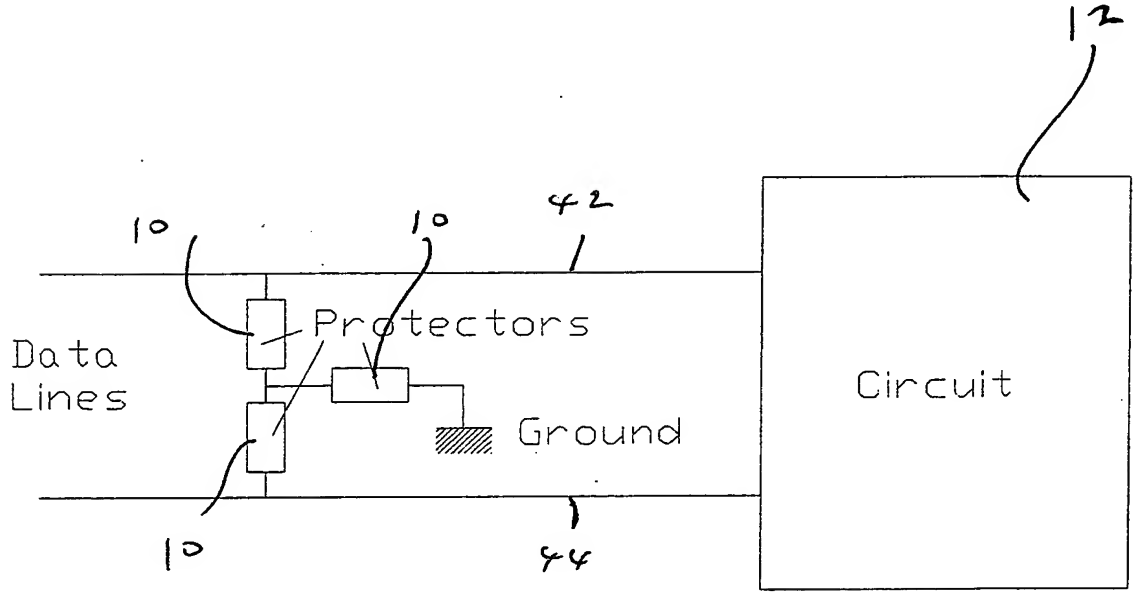
12
42
10
10
Protectors
Data Lines
Ground
Circuit
10
44

Fig 2

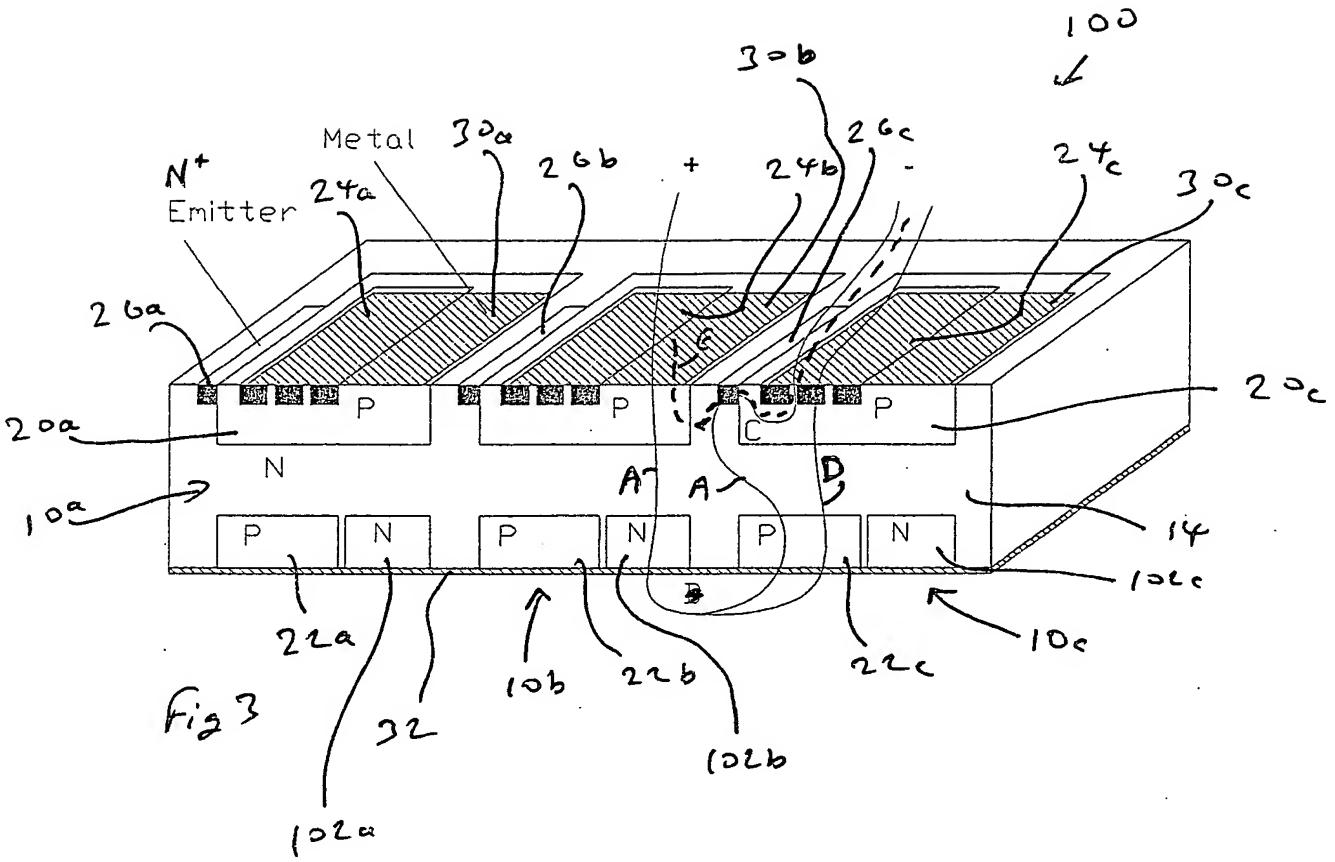
100
30b
Metal
30a
26b
+
24b
26c
-
24c
30c
N+
Emitter
24a
26a
20c
20a
P
N
10a
A
A
D
C
B
14
10c
22a
22b
22c
10b
32
102b
102a

Fig 3

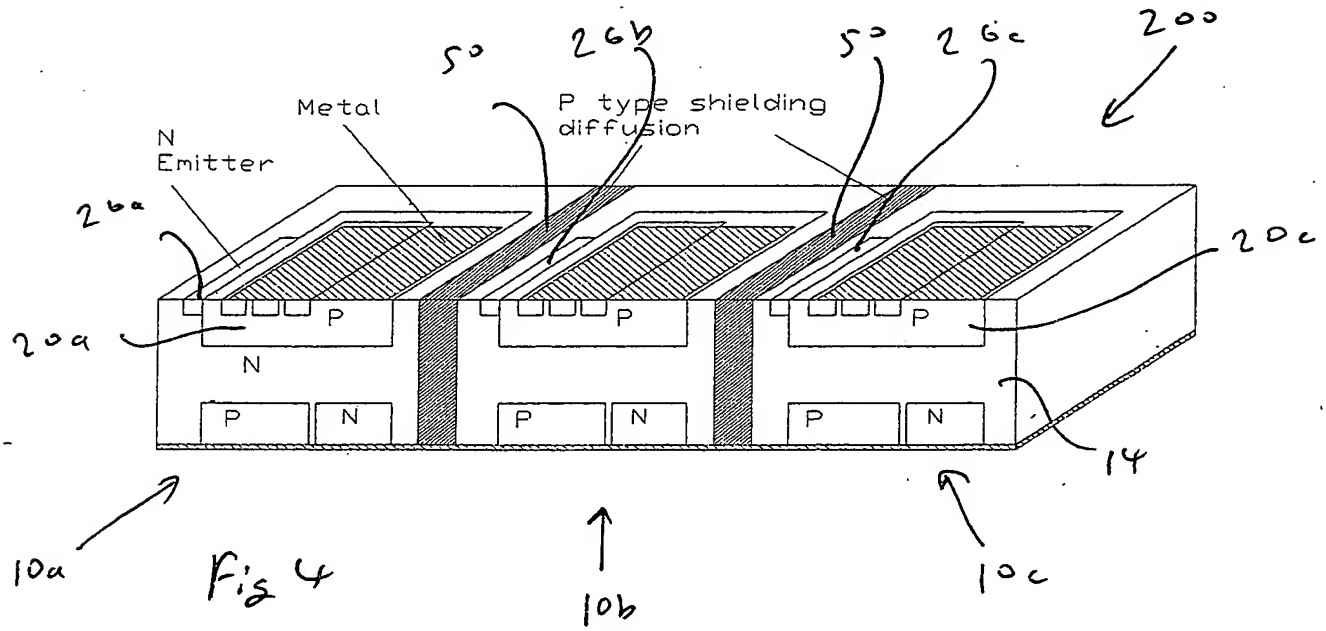
200
50
26b
50
26c
Metal
P type shielding
diffusion
N
Emitter
26a
20c
20a
P
N
14
10a
10b
10c

Fig 4